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(54) MOS transistor and fabrication process therefor

(57) An MOS transistor comprises a semiconductor substrate having a field region; a gate electrode (19) formed on the semiconductor substrate (1) through the intermediary of a gate insulating film; and source/drain regions (31) formed in the semiconductor substrate; wherein the field region including at least a lower insulating film (3,2) and an upper insulating film (4) made of a material permitting the upper insulating film to be selectively etched with respect to the lower insulating film; the gate electrode being configured such that the gate length of a top surface thereof is greater than the gate

length of a bottom surface thereof facing a channel region positioned between the source/drain regions; the gate electrode having a sidewall spacer (16) formed of a sidewall insulating layer made of the lower insulating film (3,2) and a material (16a,15) permitting the sidewall insulating layer to be selectively etched with respect to the upper insulating film, the sidewall spacer contacting a side wall of the gate electrode for covering an outer periphery of the channel region; and the channel region being substantially leveled with the source/drain regions.

Fig. 1(a)

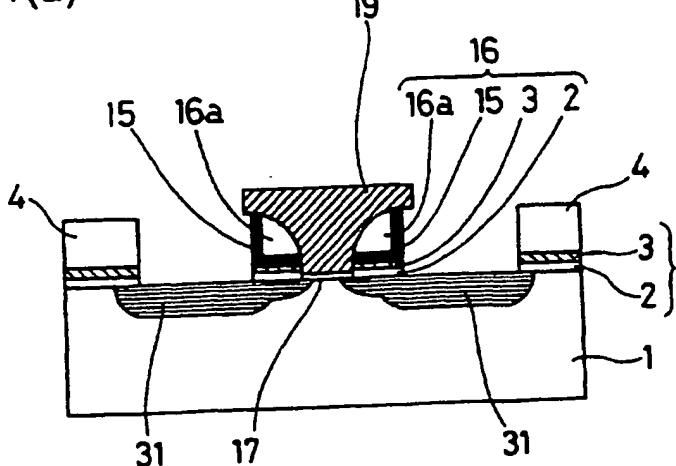
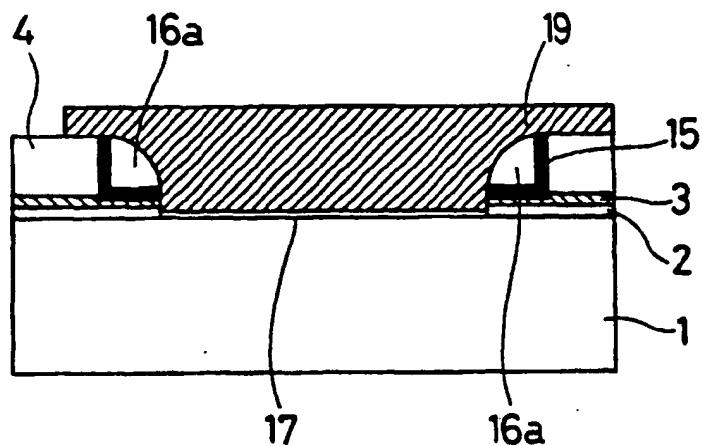


Fig. 1(b)





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EUROPEAN SEARCH REPORT

Application Number
EP 96 30 5957

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
Y	HIRONORI TSUKAMOTO ET AL: "SUB 0.1 M NMOSFET UTILIZING NARROW TRENCH GATE AND SELECTIVE EXCIMER LASER ANNEALING (SELA)" INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 29 August 1993, pages 26-28, XP000409365 * the whole document *	1-3,5	H01L29/78 H01L21/336 H01L29/423 H01L21/265 H01L27/092 H01L21/8238 H01L21/762
Y	PATENT ABSTRACTS OF JAPAN vol. 012, no. 246 (E-632), 12 July 1988 -& JP 63 036564 A (NEC CORP), 17 February 1988 * abstract; figure 2 *	1-3,5	
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A	US 5 270 234 A (HSU LOUIS L ET AL) 14 December 1993 * figures 1-10 *	1-3,5	
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A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 218 (E-761), 22 May 1989 -& JP 01 030270 A (FUJITSU LTD), 1 February 1989 * abstract; figure 1 *	6	H01L
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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search		Examiner
THE HAGUE	7 December 1998		Gélibart, J
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone	T : theory or principle underlying the invention		
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.)						
A	DE 44 15 137 C (GOLD STAR ELECTRONICS) 20 July 1995 * figure 2 *	1,6							
A	US 5 342 803 A (SHIMOJI NORIYUKI) 30 August 1994 * figure 1 *	1							
A	US 4 942 448 A (TSUKAMOTO KATSUHIRO ET AL) 17 July 1990 * figure 12 *	1							
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<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 33%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>7 December 1998</td> <td>Gélibart, J</td> </tr> </table> <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>				Place of search	Date of completion of the search	Examiner	THE HAGUE	7 December 1998	Gélibart, J
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